

features described herein may be implemented in multiple circuit units (e.g., chips), or the features may be combined in circuitry on a single chipset, as shown on FIG. 8.

[0140] FIG. 8 shows a schematic diagram of a data processing system, according to certain embodiments, for performing the functions of the exemplary embodiments. The data processing system is an example of a computer in which code or instructions implementing the processes of the illustrative embodiments may be located.

[0141] In FIG. 8, data processing system 800 employs a hub architecture including a north bridge and memory controller hub (NB/MCH) 825 and a south bridge and input/output controller hub (SB/ICH) 820. The central processing unit (CPU) 830 is connected to NB/MCH 825. The NB/MCH 825 also connects to the memory 845 via a memory bus, and connects to the graphics processor 850 via an accelerated graphics port (AGP). The NB/MCH 825 also connects to the SB/ICH 820 via an internal bus (e.g., a unified media interface or a direct media interface). The CPU Processing unit 830 may contain one or more processors and even may be implemented using one or more heterogeneous processor systems.

[0142] For example, FIG. 9 shows one implementation of CPU 830. In one implementation, the instruction register 938 retrieves instructions from the fast memory 940. At least part of these instructions are fetched from the instruction register 938 by the control logic 936 and interpreted according to the instruction set architecture of the CPU 830. Part of the instructions can also be directed to the register 932. In one implementation the instructions are decoded according to a hardwired method, and in another implementation the instructions are decoded according to a microprogram that translates instructions into sets of CPU configuration signals that are applied sequentially over multiple clock pulses. After fetching and decoding the instructions, the instructions are executed using the arithmetic logic unit (ALU) 934 that loads values from the register 932 and performs logical and mathematical operations on the loaded values according to the instructions. The results from these operations can be feedback into the register and/or stored in the fast memory 940. According to certain implementations, the instruction set architecture of the CPU 830 can use a reduced instruction set architecture, a complex instruction set architecture, a vector processor architecture, a very large instruction word architecture. Furthermore, the CPU 830 can be based on the Von Neuman model or the Harvard model. The CPU 830 can be a digital signal processor, an FPGA, an ASIC, a PLA, a PLD, or a CPLD. Further, the CPU 830 can be an x86 processor by Intel or by AMD; an ARM processor, a Power architecture processor by, e.g., IBM; a SPARC architecture processor by Sun Microsystems or by Oracle; or other known CPU architecture.

[0143] Referring again to FIG. 8, the data processing system 800 can include that the SB/ICH 820 is coupled through a system bus to an I/O Bus, a read only memory (ROM) 856, universal serial bus (USB) port 864, a flash binary input/output system (BIOS) 868, and a graphics controller 858. PCI/PCIe devices can also be coupled to SB/ICH 888 through a PCI bus 862.

[0144] The PCI devices may include, for example, Ethernet adapters, add-in cards, and PC cards for notebook computers. The Hard disk drive 860 and CD-ROM 866 can use, for example, an integrated drive electronics (IDE) or

serial advanced technology attachment (SATA) interface. In one implementation the I/O bus can include a super I/O (SIO) device.

[0145] Further, the hard disk drive (HDD) 860 and optical drive 866 can also be coupled to the SB/ICH 820 through a system bus. In one implementation, a keyboard 870, a mouse 872, a parallel port 878, and a serial port 876 can be connected to the system bus through the I/O bus. Other peripherals and devices that can be connected to the SB/ICH 820 using a mass storage controller such as SATA or PATA, an Ethernet port, an ISA bus, a LPC bridge, SMBus, a DMA controller, and an Audio Codec.

[0146] Moreover, the present disclosure is not limited to the specific circuit elements described herein, nor is the present disclosure limited to the specific sizing and classification of these elements. For example, the skilled artisan will appreciate that the circuitry described herein may be adapted based on changes on battery sizing and chemistry, or based on the requirements of the intended back-up load to be powered.

[0147] The functions and features described herein may also be executed by various distributed components of a system. For example, one or more processors may execute these system functions, wherein the processors are distributed across multiple components communicating in a network. The distributed components may include one or more client and server machines, which may share processing, as shown by FIG. 10, in addition to various human interface and communication devices (e.g., display monitors, smart phones, tablets, personal digital assistants (PDAs)). The network may be a private network, such as a LAN or WAN, or may be a public network, such as the Internet. Input to the system may be received via direct user input and received remotely either in real-time or as a batch process. Additionally, some implementations may be performed on modules or hardware not identical to those described. Accordingly, other implementations are within the scope that may be claimed.

[0148] The above-described hardware description is a non-limiting example of corresponding structure for performing the functionality described herein.

[0149] Obviously, numerous modifications and variations of the present disclosure are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

1. A burner system for clean combustion in gas turbines, comprising:

- an air manifold having an air inlet for receiving pressurized air;
- a combustor including a first shell surrounding a plurality of air tubes, wherein each air tube is connected to the air manifold, wherein the combustor is configured to burn a mixture of fuel, carbon dioxide (CO₂) and oxygen (O₂), wherein burning the mixture heats the pressurized air in the air tubes, the combustor further including a combustion outlet port, at least one igniter and at least one thermocouple;
- a headend connected to the combustor, the headend including a second shell surrounding a plurality of ceramic ion transfer membrane (ITM) tubes equally spaced longitudinally within the headend, wherein each air tube is further connected to an air space in the